SYN2000SMPLL1

rev_0	initial rev
rev_1	clarify PN

	MIN	TYP	MAX	UNITS	NOTES	Production Test	First Article Test
Frequency		2000		MHz	1	..	..
PD Frequency		20		MHz	1	..	..
Lock Time (within 1KHz)			20	msec	3	..	..
Reference Frequency (external)		20		MHz		..	..
Output Power (sinewave)	0	3	6	dBm	1	..	..
Output Impedance		50		ohms			
Phase Noise @							
10 KHz Offset		-115		dBc/Hz	1	..	..
100 KHz Offset		-136		dBc/Hz	1	..	..
1MHz Offset		-156		dBc/Hz	1	..	..
Spurious			-60	dBc	3	..	..
Harmonics		-15	-10	dBc	3	..	..
Vcc		4.2		V	5	..	..
Icc		50		mA	1	..	..
Operating Temperature	-40		+85	C	3	..	..
Package							
Length		0.500	0.504	inch	5	..	..
Width		0.500	0.504	inch	5	..	..
Height		0.106	0.110	inch	5	..	..
Programming		i^2c or spi			7		

Notes

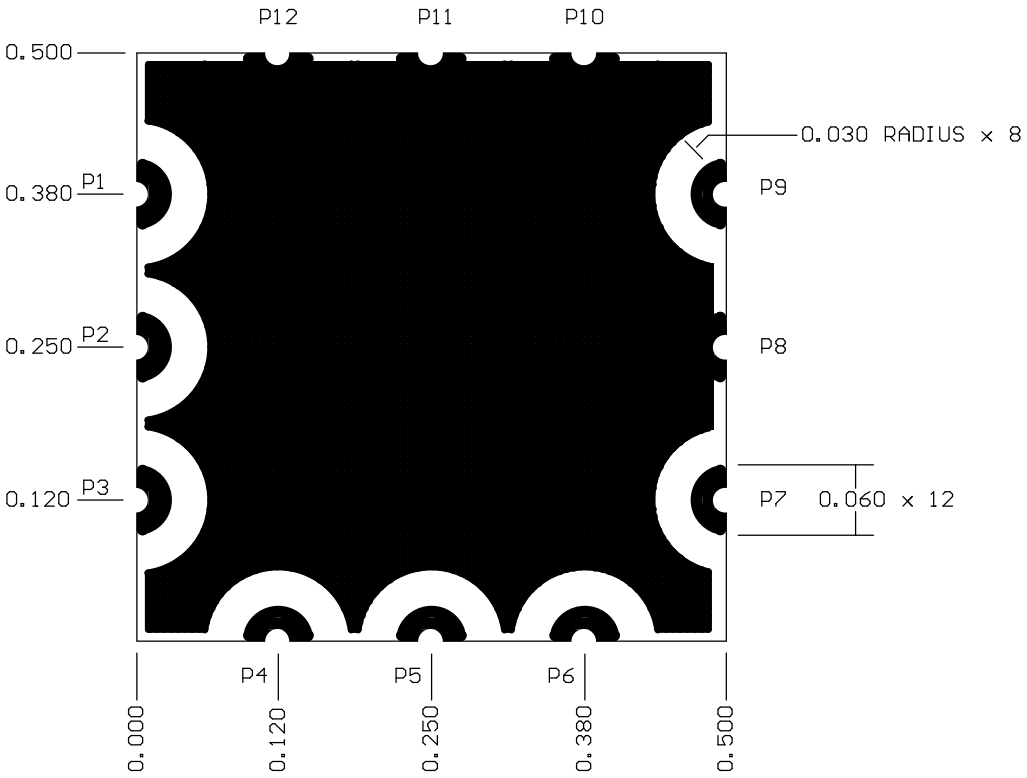
1. Tested in production, and guaranteed
2. Per current design, not a tested parameter
3. Sample tested from production lot and guaranteed
4. Not a tested or guaranteed design goal
5. By inspection
6. Design goal subject to change
7. ADF4106 or equivalent

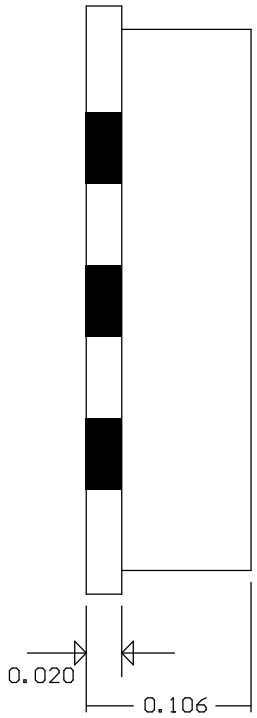
sig **date**

sig **date**

PLL-SM1 FOOTPRINT

TOP VIEW, BOT SIDE





P1 = RF OUT

P2 = REF IN

P3 = CLOCK

P4 = DATA

P5 = LOAD ENABLE

P6 = LOCK DETECT

P7 = VCC

P8 = GROUND

P9 = OPEN

P10-12 = GROUND